ABSTRACT OF THE DISCLOSURE

A switching node (20) has a semiconductor switch core (22) and plural switch port devices (24). The semiconductor switch core comprises a two dimensional buffer matrix having one buffer memory (40) per crosspoint to which cells having differing priority classes are written. The switch core further has plural switch core ports (30), with each of the switch core ports writing traffic cells to a row (42) of the matrix and reading traffic cells from a column (44) of the matrix. For each crosspoint of the matrix a high priority signaling element (46H) is formed in the semiconductor switch core. A novel low priority cell flushing operation the present invention moots any cell blocking problems.